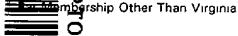


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Date: August 28, 2001

Attorney Docket No. ASA-1026



24956

PATENT TRADEMARK OFFICE

To: Assistant Commissioner for Patents
 Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of:

Inventor: K. WATANABE et al (see attached)

For:

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING
 A SELF-TESTING FUNCTION

jc857 U.S. PTO
 09/939589
 08/28/01

Enclosed are:



6 Sheets of Drawings



This application is being filed without an executed Declaration.



Priority is claimed from Japanese Application No. 2000-298525
 filed September 29, 2000. A certified copy is attached herewith.



Copies of the disclosure documents listed on the attached PTO 1449 form and
 discussed in the specification or attached Information Disclosure Statement.



A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.



Specification: Abstract , Description 30 pages; and 6 claim(s).



Preliminary Amendment.



Executed Declaration.

The filing fee is calculated as shown below:

For:	No. Filed	No. Extra
Basic Fee		
Total Claims	6 -20 =	* 0
Indep Claims	1 - 3 =	* 0
<input type="checkbox"/> Multiple Dependent Claim (s)		

* If difference is less than zero
 then enter '0' in second column

Rate	Fee
	\$ 355
x 9	\$
x 40	\$
+ 135	\$
Total	\$

OR

Rate	Fee
	\$ 710
x 18	\$ 0
x 80	\$ 0
+ 270	\$ 0
Total	\$ 710



A check in the amount of \$ 710.00 is enclosed for the filing fee.



The Commissioner is hereby authorized to charge any additional fees that may be required to
 Deposit Account No. 50-1417.

Respectfully Submitted,

By: 
 John R. Mattingly
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